Sub-THz Wireless Communication & Sensing
– A Perspective on Device, Circuit, and System

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Outline

• Overview of a few Sub-THz applications and Technical challenges
• Status of Power Amplifier capabilities on different Semiconductor platforms
• Examples of System level performance for different sub-THz applications
• State-of-the-art capabilities of different Silicon Technologies and roadmap
• Summary
System Applications in Sub-THz Frequency Bands

- **Communication**
  - 16 QAM / 80Gb/s
  - EVM=12% rms
  - [S. Lee, et al, ISSCC, 2019.]
  - Giant High Data-Rate

- **Radar**
  - [J. Grzyb, et al, TTST, 2016.]
  - Super High Resolution and 3D Imaging

- **Imaging**
  - Super High Resolution and Hyperspectral

- **Spectroscopy**
  - High Sensitivity and Molecular Signature
Major Technical Challenges

- **Challenge 1**
  **Signal Propagation**: Path loss at sub-THz

- **Challenge 2**
  **Device Capabilities**: Limited gain, power density, $P_{\text{out}}$, and NF

- **Challenge 3**
  **Array Pitch Size**: Small element pitch for 2D arrays ($\lambda/2=625\mu$m at 240GHz)

- **Challenge 4**
  **Systems/Circuits**: Limited gain, power density, freq. $\Rightarrow$ Nonlinear circuits
Power Amplifier Survey (2000-present) by Georgia Tech GEMS Group

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- Output power vs. frequency
- Power generation scheme vs. frequency
- Power amplifiers and Fundamental Oscillators (~200GHz)
- Multipliers and Harmonic Oscillators (~500GHz and above)

$f_T$ and $f_{\text{max}}$ of Existing Device Technologies

- **$f_T$ cut-off frequency**: Transistor short-circuit ac current gain falls to 1
  - Switching circuits MUX/dividers and low noise circuit LNA

- **$f_{\text{max}}$ max oscillation frequency**: Transistor maximum unilateral power gain falls to 1
  - Power amplifiers, LNAs, general amplifiers, oscillators

- **Amplifier design Rule of Thumb**: Frequency $f < f_{\text{max}}/2$ with ~6dB gain for perfectly neutralized devices

\[ f_T = \frac{g_m}{2\pi C_{gg}} \]

\[ f_{\text{max}} \approx \frac{f_T}{\sqrt{8\pi R_g C_{gd}}} \]

**III-V Technology**

- Teledyne InP 130nm ($f_{\text{max}} = 1.1$THz)
- Teledyne InP 250nm ($f_{\text{max}} = 750$GHz)
- Keysight InP 500nm ($f_{\text{max}} = 550$GHz)
- Qorvo GaN 150nm ($f_{\text{max}} = 110$GHz)
Squeezing More Power Gain from Devices

Maximum available gain:
\[ G_{ma} = \left| \frac{Y_{21}}{Y_{12}} \right| (K - \sqrt{K^2 - 1}) \]

Maximum stable gain (stabilized device, K=1):
\[ G_{ms} = \left| \frac{Y_{21}}{Y_{12}} \right| \]

Stability factor:
\[ K = \frac{2 \text{Re}(Y_{11}) \text{Re}(Y_{22}) - \text{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} \]

Unilateral power gain (U):
\[ U = \frac{|Y_{21} - Y_{12}|^2}{4[\text{Re}(Y_{11}) \text{Re}(Y_{22}) - \text{Re}(Y_{12}) \text{Re}(Y_{21})]} \]
\[ = \frac{4[\text{Re}(Y'_{11}) \text{Re}(Y'_{22})]}{|Y_{21}'|^2} \]

Maximum achievable gain:
\[ G_{max} = (2U - 1) + 2\sqrt{U(U - 1)} \approx 4U \]

Achievable Power Gain in Example CMOS Technology vs. Teledyne 250nm InP

- Device with layout and parasitics extraction
- Basic device vs. Neutralization vs. Embedding (100GHz-300GHz)
- An example CMOS technology ($f_{\text{max}} \sim 280$GHz) vs. Teledyne 250nm InP ($f_{\text{max}} \sim 750$GHz)
Applications and Systems at Sub-THz (Communication)

- A 240-GHz transceiver front-end with antenna using IHP SiGe:C SiGe BiCMOS
- TX sat. $P_{out}$ of -0.8 dBm with optical lens for wireless transmission over 15 cm
- 25 Gb/s BPSK with BER of $2.2 \times 10^{-4}$.

Applications and Systems at Sub-THz (Communication)

- A 300GHz-Band Single-Chip CMOS Transceiver using 40nm CMOS
- Power mixer + double-rat-race 4-way combiner $\rightarrow$ TX sat. $P_{\text{out}}$ of -1.6dBm
- Mixer-first receiver $\rightarrow$ 20dB NF
- 80Gb/s 16QAM over 3cm

Applications and Systems at Sub-THz (Imaging)

- A 100GHz-300GHz Continuous-Wave Hyperspectral Imaging Transceiver (Globalfoundries 45nm CMOS SOI)
- Transmission mode imaging by step-motor-controlled 2D translation stage
- Non-contact screening for food safety and 3D printing products

- Cookie and metal screw in a translucent package

- Dried and fresh leaves

Applications and Systems at Sub-THz (Imaging)

- **RX**: Broadband 115-to-325GHz 4th-subharmonic mixer (SHM)
  - TX: Broadband 90-to-300GHz distributed quadrupler (DQ)

Applications and Systems at Sub-THz (Radar)

- A 145GHz FMCW-Radar Transceiver in 28nm bulk CMOS
- High RF carrier permits greater velocity and MIMO-angular resolution
- A wide RF bandwidth of 13GHz → 11mm range/depth resolution

Applications and Systems at Sub-THz (Spectroscopy)

- A 220-to-320GHz Spectrometer for Molecular Gas Spectroscopy (65nm CMOS)
- Frequency doubler array + on-chip folded slot antenna array
- 5.2mW Radiated Power and 14.6-to-19.5dB Noise Figure

Frontend Circuits at Sub-THz (Power Generation/TX)

- **215 GHz Harmonic Oscillator in TMSC 65nm CMOS**
- Max dc-to-RF efficiency of 4.6% at 215 GHz and max $P_{\text{out}}$ of 5.6 dBm from a single oscillator

Frontend Circuits at Sub-THz (Power Generation/TX)

- 500 GHz Sub-harmonic Oscillator in Globalfoundries 9HP SiGe
- Multi-concentric-ring structure for multi-phase injection-locking multiplier
- Max $P_{\text{out}}$ of -16.6 dBm at 498 GHz with 5.1% freq. tuning and phase noise of 87 dBc/Hz at 1 MHz offset

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Frontend Circuits at Sub-THz (Regenerative RX and Harmonic Oscillator TX)

- **Harmonic-oscillator TX** and Regenerative RX with on-chip TDC for digitized RX outputs
- Operating at 320GHz using Globalfoundries 45nm CMOS SOI
- On-chip multi-feed slot antenna for on-antenna power combining

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity (dBm)</td>
<td>-89</td>
</tr>
<tr>
<td>Max Comm. Distance (cm)</td>
<td>50</td>
</tr>
<tr>
<td>Data Rate, Type, BER</td>
<td>4.4Mb/s OOK, 10^{-7}</td>
</tr>
<tr>
<td>TX EIRP (dBm)</td>
<td>-11.6</td>
</tr>
<tr>
<td>$P_{DC}$ (mW)</td>
<td>18.2/31.1 (TX/RX)</td>
</tr>
</tbody>
</table>

[T. Chi, H. Wang, M.-Y. Huang, F. F. Dai, and H. Wang, “A bidirectional lens-free digital-bits-in/-out 0.57mm2 terahertz nano-radio in CMOS with 49.3mW Peak power consumption supporting 50cm Internet-of-Things communication,” 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018.] Georgia Tech, US
CMOS Cut-off Frequency $f_T$

- Transistor speed metric
  - Particularly relevant for switching circuits such as MUX/DMUX, dividers, etc
  - Definition: Frequency at which short-circuit ac current gain falls to 1
- CMOS $f_T$ increases with scaling

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = |g_m Z_{\text{in}}| = \left| g_m \left( \frac{1}{j\omega C_{\text{in}}} \right) \right| = 1
\]

\[
\Rightarrow \omega_T = \frac{g_m}{C_{\text{in}}}
\]

\[
f_T = \frac{g_m}{2\pi C_{gg}}
\]

### Scaling

<table>
<thead>
<tr>
<th>Long channel</th>
<th>Short channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_T \propto$</td>
<td>$f_T \propto$</td>
</tr>
<tr>
<td>$W/L_g$</td>
<td>$W/L_g$</td>
</tr>
<tr>
<td>$W/2L_g$</td>
<td>$W/L_g$</td>
</tr>
<tr>
<td>$1/L_g^2$</td>
<td>$1/L_g$</td>
</tr>
</tbody>
</table>

CMOS Maximum Oscillation Frequency $f_{\text{MAX}}$

- Transistor speed metric
  - Particularly relevant for circuits that generate power such as LNA’s, PA’s, VGA’s, etc
  - Definition: Frequency at which the maximum unilateral power gain equals 1
  - Parasitics have a larger impact at smaller dimensions, which limits $f_{\text{MAX}}$ in advanced CMOS nodes.

Conjugate match at the input:

- $R_S = R_g$
- $i_{\text{in}} = i_{\text{ins}} = V_S / 2R_g$
- $Z_{\text{in}} = R_g + \frac{1}{j\omega C_{gs}} \approx R_g$

Conjugate match at the output:

- $R_L = Z_{\text{out}}$
- $Z_{\text{out}} = \frac{1}{g_m C_{gd} + C_{gs} + C_{gd}}$
- $= \frac{1}{g_{ds} + 2\pi f T C_{gd}}$
- $G_P = \frac{G_{\text{out}}}{G_{\text{in}}} = \frac{\frac{1}{2}i^2_{\text{out}} R_{\text{out}}}{\frac{1}{2}i^2_{\text{in}} R_{\text{in}}} = \frac{1}{4} \left( \frac{i_{\text{os}}}{i_{\text{ins}}} \right)^2 \frac{R_L}{R_g} = \frac{1}{4} \left( \frac{f_T}{f} \right)^2 \frac{R_L}{R_g}$
- $|G_P| = 1 \Rightarrow f_{\text{max}} = \frac{1}{2} f_T \sqrt{\frac{R_L}{R_g}}$
- $\therefore f_{\text{max}} = \frac{f_T}{2\sqrt{g_{ds} R_g + 2\pi f_T R_g C_{gd}}}$
- $f_{\text{max}} \approx \frac{f_T}{\sqrt{8\pi R_g C_{gd}}}$

Scaling of $f_{\text{max}}$ depends on $f_T$, $R_g$, and $C_{gd}$

References:
CMOS $f_{\text{MAX}}$ peaks at $\approx 450\text{GHz}$

- Advanced nodes struggle with gate and interconnect resistance

- Peak $f_{\text{MAX}}$ achieved in the 32nm – 22nm nodes

H. J. Lee et al, “Intel 22nm FinFET (22FFL) Process Technology for RF and mmWave Applications and Circuit Design Optimization for FinFET Technology“, IEDM 2018
SiGe $f_T$, $f_{\text{MAX}}$

- $f_T$ improves with vertical scaling $f$

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_C + \tau_B + \tau_{\text{CSCL}} = \frac{kT}{qI_C} C_{EB} + \left( \frac{kT}{qI_C} R_C + R_E \right) C_{CB} + \frac{W_B^2}{\gamma D_n} + \frac{W_{\text{CSCL}}}{2v_{\text{SAT}}},$$

- $f_{\text{MAX}}$ improves with reduction in dominant parasitics

$$f_{\text{MAX}} = \sqrt{\frac{f_T}{8\pi R_B C_B}}$$

- Reduce transit time, increase $f_T$

- Vertical scaling with lateral scaling maintains constant current / device length for self-heating and current delivery

- Reduce $C_{\text{cb}}$ intrinsic and extrinsic base capacitance while maintaining low base resistance

- Reduce $R_B$ extrinsic and intrinsic resistances while maintaining narrow base width

- Emitter shrinks with increasing current density
Advances in SiGe have reached 500GHz $f_T$ / 700GHz $f_{\text{MAX}}$
European Consortia for Advanced SiGe Development

• Four projects funded by EU for over a decade
• Significant achievement in both pushing SiGe HBT performance and BiCMOS integration
  • DOT5, 2008 – 2010, 500GHz SiGe HBT
  • RF2THZ, 2011 – 2014, 55nm SiGe BiCMOS
  • DOT7, 2012 – 2016, 700GHz SiGe HBT
  • TARANTO, 2017 – 2020, 700GHz SiGe HBT, 130-28nm SiGe BiCMOS
Amplifier Power and Gain at 250GHz with 500GHz SiGe

M. Eissa and D. Kissinger, “A 13.5dBm Fully Integrated 200-to-250GHz Power Amplifier with a 4-Way Power Combiner in SiGe:C BiCMOS”, ISSCC 2019

Single Unit Power Amplifier
- Cascode PA unit, bias circuit and load pulling simulation
- Maximum $P_{\text{sat}} = 11$ dBm
- Output impedance as compromise between $P_{\text{sat}}$ and $S_{22}$

4-way Zero-Degree Power Amplifier
- Simulated gain and output 1-dB compression point across process variations
Summary

• Sub-THz applications reviewed
  • Communications – higher data rate
  • Radar – higher resolution
  • Imaging – high resolution and hyperspectral
  • Spectroscopy – high sensitivity and molecular signature

• Challenges for device, circuit and systems at sub-THz frequencies
  • Signal propagation and path loss at sub-THz
  • Device and circuit issues – limited gain, power density, Pout, NF
  • Array pitch size

• Semiconductor technology
  • Higher ft/fmax technology needed for sub-THz
    • fmax > 2x f application rule of thumb
  • CMOS fmax limited by parasitics (gate, interconnect R) for advanced node CMOS
  • SiGe demonstrated path to 500GHz/700GHz ft/fmax
  • Initiatives in US and Europe for development of 700GHz SiGe BiCMOS technology